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IN-PIXEL MEMORY FOR DISPLAY DEVICES

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DESCRIPTION

The present invention relates to in-pixel memories and in-pixel memory circuits, particularly for display devices. The present invention is particularly suited to, but not limited to, providing in-pixel memory circuits in active matrix liquid crystal display devices.

Known display devices include liquid crystal, plasma, polymer light emitting diode, organic light emitting diode, and field emission. Such devices comprise an array of pixels, usually in rows and columns. In active matrix display devices, each pixel is typically associated with one or more respective switching devices, such as thin film transistors, to provide an array of pixels and switching devices. In operation, the pixels are addressed according to an addressing scheme in which each pixel is regularly refreshed for each frame to be displayed with display data (e.g. video) specifying the intensity level the pixel is to display. Usually the addressing scheme selects the pixels on a row-by-row basis and provides individual intensity levels on a column-by-column basis.

One development in the field of display devices is to provide in-pixel memories, whereby a respective memory device is provided for each pixel, the memory devices being arranged in an array corresponding to the pixel array. Static images may then be displayed without a need to refresh, thereby saving power. This is potentially particularly attractive for display devices for portable devices such as mobile telephones, cordless telephones, personal digital assistants, and so on.

It is known to use static random access memory (SRAM) and dynamic random access memory (DRAM) circuits for such in-pixel memory. Conventionally only one memory device (formed by a circuit) is provided for each pixel. A separate array of SRAM or DRAM circuits is provided in addition

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BRIEF DESCRIPTION OF THE DRAWINGS.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic illustration (not to scale) of a liquid crystal display device;

Figure 2 is a schematic illustration of a sample 2x2 portion of an array of pixels;

Figure 3 is a schematic illustration of a simple MRAM stack;

Figure 4 is a circuit diagram of an in-pixel memory circuit;

Figure 5 shows a pixel and in-pixel memory arrangement including two MRAMs, a read-out circuit and a drive circuit;

Figure 6 shows a schematic diagram, not to scale, of a constructional layout employed for a pixel;

Figure 7 is a flowchart showing certain process steps used to form an in-pixel memory structure;

Figure 8 shows a cross-section between points X-X indicated in Figure 6;

Figure 9 shows a preferred MRAM stack in cross-section (not to scale); and

Figures 10 and 11 show the results of simulations performed for the in-pixel memory circuit described with reference to Figure 4.

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Figure 1 is a schematic illustration (not to scale) of a liquid crystal display device 1, comprising two opposed glass plates 2, 4 (or any other suitable transparent plates). The glass plate 2 has an active matrix layer 6, which will be described in more detail below, on its inner surface, and a liquid crystal orientation layer 8 deposited over the active matrix layer 6. The opposing glass plate 4 has a common electrode 10 on its inner surface, and a liquid crystal orientation layer 12 deposited over the common electrode 10. A liquid crystal layer 14 is disposed between the orientation layers 8, 12 of the two glass plates. Except for any active matrix details described below, in